an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom;

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom; and

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a shared operand unit coupled to the first MAC unit and the second MAC unit for providing a shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other.

2. The integrated circuit according to claim 1 wherein said array processor uses a simplified IEEE floating point notation which excludes said IEEE floating point exceptions, comprising underflow, overflow, divide by zero, inexact, and invalid.

3. The integrated circuit according to claim 1 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and the array processor.

4. The integrated circuit according to claim 3 wherein said wire bundle comprises at least 256 wires.

5. The integrated circuit according to claim 1 wherein the MAC unit comprises a computational unit that multiplies a first operand by a second operand to obtain a result and then adds or subtracts from the result a third operand, wherein the operands are either scalars or vectors.

6. The integrated circuit according to claim 1 further comprising

a global external bus unit for providing an interface between the integrated circuit and the external environment, the global external bus unit coupled to the embedded microprocessor by a system bus and by a separate dedicated bus.

7. The integrated circuit according to claim 1 wherein the array processor performs a plurality of vector operations selected from a group consisting of addition of a plurality of vectors and multiplying a vector by a scalar.

8. (CANCELED)

9. A method using an array processor for frame rendering and DSP applications, comprising:

determining a fixed point result by performing a fixed point addition or subtraction on a plurality of fixed point operands;

converting the fixed point result to a first floating point result; and

determining a second floating point result by performing a floating point multiplication and then accumulation on the first floating point result and a plurality of floating point operands.

REMARKS

Claims 1-9 are pending. Claim 9 was withdrawn from consideration by the Examiner. Claims 1-8 were rejected under 35 U.S.C. §103(a) as being obvious in view of Ngai et al., (U.S. Pat. No. 4,888,682, hereinafter referred to as "Ngai") and Wang et al., (U.S. Pat. No. 5,187,796, hereinafter referred to as "Wang"). Claim 8 has been canceled.

Restriction under 35 U.S.C. §121

The Examiner divided claims 1- 9 into two Groups: Group I included claims 1-8, and group II claim 9. Under MPEP §806.05(e) the Examiner asserted that the process of Group II "clearly does not require the specific structure of the apparatus recited in the claims of Group I." Applicant respectfully traverses the requirement to restrict.